

DMA SCHEDULING MECHANISM

ABSTRACT

5 The present invention is directed to methods and systems for implementing a
DMA scheduling mechanism and a DMA system for transmission from fragmented
buffers. According to an aspect of the present invention, a processor controls several
devices via a polled interface to interleave DMA data transfers on different Input/Output
(I/O) ports in an efficient manner. According to another aspect of the present invention, a
system for handling transmission of network packets which are assembled from multiple
10 memory buffers with different octet alignments is provided. The hardware/software
combination allows efficient joining of packet fragments with differing octet alignments
when the underlying memory system is word based, and further allows insertion of other
data fields generated by a processor.